WHAT IS CLAIMED IS :

1. A method for reducing an importance level of a line in a memory of a cache, the method comprising providing an instruction to the cache indicating that the line is a candidate for replacement.

2. The method as recited in claim 1 further comprising reducing an importance level of the line based on the instruction.

3. The method as recited in claim 2 wherein the reducing of the importance level of the line results in the line being replaced prior to another line scheduled for replacement by a replacement policy of the cache.

4. The method as recited in claim 3 wherein the replacement policy is a least recently used policy and wherein the other line is less recently used than the line.

5. The method as recited in claim 1 further comprising altering an allocation methodology of the cache based on the instruction.

6. The method as recited in claim 1 wherein the instruction in part of an application kernel.

7. The method as recited in claim 1 wherein the instruction is generated by a compiler.

8. The method as recited in claim 1 wherein the instruction is an extension of a memory access instruction.

9. A instruction for increasing hit rate of a cache, the instruction comprising an indication that a line in a memory of the cache is a candidate for replacement.

10. The instruction as recited in claim 9 wherein the indication causes a reduction of an importance level of the line.

11. The instruction as recited in claim 10 wherein the reducing of the importance level of the line results in the line being replaced prior to another line scheduled for replacement by a replacement policy of the cache.

12. The instruction as recited in claim 11 wherein the replacement policy is a least recently used policy and wherein the other line is less recently used than the line.

13. The instruction as recited in claim 9 further comprising altering an allocation methodology of the cache based on the instruction.

14. The instruction as recited in claim 9 wherein the instruction in part of an application kernel.

15. The instruction as recited in claim 9 wherein the instruction is generated by a compiler.

16. The instruction as recited in claim 9 wherein the instruction is an extension of a memory access instruction.

17. An article comprising a storage medium, the storage medium having a set of instructions, the set of instructions being capable of being executed by at least one processor to implement a method for reducing an importance level of a line in a memory of

a cache, the set of instructions when executed comprising providing an indication to the cache that the line is a candidate for replacement.

18. The article as recited in claim 17 wherein the set of instructions further comprises reducing an importance level of the line based on the indication.

19. The article as recited in claim 18 wherein the reducing of the importance level of the line results in the line being replaced prior to another line scheduled for replacement by a replacement policy of the cache.

20. The article as recited in claim 19 wherein the replacement policy is a least recently used policy and wherein the other line is less recently used than the line.

21. The article as recited in claim 17 further comprising altering an allocation methodology of the cache based on the indication.

22. The article as recited in claim 17 wherein the indication is part of an application kernel.

23. The article as recited in claim 17 wherein the indication is generated by a compiler.

24. The article as recited in claim 17 wherein the indication is an extension of a memory access instruction.

25. A cache comprising:

a cache memory including a cache line; and

a cache control logic for reducing an importance level of the cache line based on an instruction.

26. The cache as recited in claim 25 wherein the instruction provides an indication that the cache line is a candidate for replacement.

27. The cache as recited in claim 26 wherein the cache control logic reduces an importance level of the cache line based on the indication.

28. The cache as recited in claim 27 wherein the reducing of the importance level of the cache line results in the cache line being replaced prior to another cache line scheduled for replacement by a replacement policy of the cache.

29. The cache as recited in claim 25 further comprising altering an allocation methodology of the cache based on the instruction.

30. A method for reducing an importance level of a line in a memory of a cache, the method comprising:

providing an instruction to the cache indicating that the line is a candidate for replacement; and

reducing an importance level of the line based on the instruction.